2022 LASCAS Program Schedule

Tuesday, March 1st	
09:15-10:45	Session 1A: Tutorial 1 AM "Trends and Challenges in EDA" (chair: Ronald Valenzuela)
09:15-10:45	Session 1B: Tutorial 2 AM "Circuits for reversible computing" (chair: Gonzalo Carvajal)
09:15-10:45	Session 1C: Tutorial 3 AM "Improving integrated circuit reliability"
10:45-11:00	**Coffee Break**
11:00-12:30	Session 2A: Tutorial 1 AM "Trends and Challenges in EDA" - part 2 (chair: Ronald Valenzuela)
11:00-12:30	Session 2B: Tutorial 2 AM "Circuits for reversible computing" - part 2 (chair: Gonzalo Carvajal)
11:00-12:30	Session 2C: Tutorial 3 AM part 2 "Improving integrated circuit reliability" - part 2
12:30-14:00	**Lunch**
14:00-15:30	Session 3A: Tutorial 4 PM "Power Analysis in VLSI circuit design: An Overview"(chair: Ronald Valenzuela)
14:00-15:30	Session 3B: Tutorial 5 PM "Battery Life Extension Techniques for Energy Harvesting-Based IoT Devices" (chair: Gonzalo Carvajal)
15:30-15:45	**Coffee Break**
15:45-17:15	Session 4A: Tutorial 4 PM "Power Analysis in VLSI circuit design: An Overview" - part 2 (chair: Ronald Valenzuela)
15:45-17:15	Session 4B: Tutorial 5 PM "Battery Life Extension Techniques for Energy Harvesting-Based IoT Devices" - part 2 (chair: Gonzalo Carvajal)
19:00-21:00	**Welcome Reception**
Wednesday, March 2nd	
08:15-08:45	Session 5: **Opening Session** (chairs: Victor Grimblatt, Yann Deval)
08:45-10:00	Session 6: Keynote talk 1: **David Atienza** "Sustainable Cloud Computing Systems for a Digitalized World" (chair: Victor Grimblatt)
10:00-10:15	**Coffee Break**
10:15-11:35	Session 7A: Parallel W1A Communication Systems - Track 3 (chair: Francois Rivet)

10:15-10:35	31	Antonello Florio and Gianfranco Avitabile. Multiple Source Angle of Arrival Estimation through Phase Interferometry
10:35-10:55	61	Alexis Rodrigo Iga Jadue, Sylvain Engels and Laurent Fesquet. A Novel Event-Based Method for ASK Demodulation
10:55-11:15	44	Marcelo Santana, Thiago Mussolini and Tales Pimenta. The implementation of a Communication Circuitry for Ultra Dense EEG Networks of Active Electrodes
11:15-11:35	68	Piyush Kumar, Dario Stajic, Erkan Nevzat Isa and Linus Maurer. 26 GHz VCO in 22nm FDSOI Technology for RADAR Application
10:15-11:35	Session 7B: Parallel W1B Approximate Computing for Energy-Efficient VLSI Circuits and Systems - SS3 (chair: Jorge Castro Godinez)	
10:15-10:35	107	Patricia da Costa, Pedro T. L. Pereira, Brunno Abreu, Guilherme Paim, Eduardo Da Costa and Sergio Bampi. Improved Approximate Multipliers for Single-Precision Floating-Point Hardware Design
10:35-10:55	106	Guilherme Barbosa Manske, Clayton Rodrigues Farias, Paulo Francisco Butzen and Leomar Soares da Rosa Junior. A Fast Approximate Function Generation Method to ATMR Architecture
10:55-11:15	104	Marcio Monteiro, Ismael Seidel, Mateus Grellert, Jose Luis Güntzel, Leonardo Soares and Cristina Meinhardt. Exploring the Impacts of Multiple Kernel Sizes of Gaussian Filters Combined to Approximate Computing in Canny Edge Detection
11:15-11:35	108	Brunno Abreu, Guilherme Paim, Jorge Castro-Godínez, Mateus Grellert and Sergio Bampi. On the Netlist Gate-level Pruning for Tree-based Machine Learning Accelerators
11:40-13:00	Session 8A: Parallel W2A Nano-electronic Circuits and Systems I - Track 10 (chair: Francois Rivet)	
11:40-12:00	12	Esteban Garzón, Ramiro Taco, Luis-Miguel Procel-Moya, Lionel Trojman and Marco Lanuzza. Voltage and Technology Scaling of DMTJ-based STT-MRAMs for Energy-Efficient Embedded Memories
12:00-12:20	85	Ariana Musello, Santiago S. Pérez, Marco Villegas, Luis Miguel Prócel, Ramiro Taco and Lionel Trojman. Energy-Efficient FinFET- Versus TFET-Based STT-MRAM Bitcells
12:20-12:40	56	Kevin Vicuña, Luis Miguel Prócel, Lionel Trojman and Ramiro Taco. DMTJ-Based Non-Volatile Ternary Content Addressable Memory for Energy-Efficient High-Performance Systems
12:40-13:00	20	Olivier Bonnaud. Technical and pedagogical challenges in micro-nanoelectronics for facing up-coming digital society
11:40-13:00	Session 8B: Parallel W2B Fault Tolerant and Reliability - Track 5	
11:40-12:00	63	Chandrasekhara Srinivas Vatti, Rakesh M B, Ravi Teja Reddy P and Acharyya Amit. A hierarchical fault-tolerant and cost effective framework for RRAM based Neural Computing Systems

12:00-12:20	25	Orlando Verducci, Duarte Oliveira and Gracieth Batista. Fault-Tolerant Finite State Machine Quasi Delay Insensitive in Commercial FPGA Devices
12:20-12:40	41	Geancarlo Abich, Rafael Garibotti, Ricardo Reis and Luciano Ost. The Impact of Soft Errors in Memory Units of Edge Devices Executing Convolutional Neural Networks
12:40-13:00	57	Geancarlo Abich, Rafael Garibotti, Jonas Gava, Ricardo Reis and Luciano Ost. Impact of Thread Parallelism on the Soft Error Reliability of Convolution Neural Networks
13:00-14:40	**Lunch**	
14:40-15:50	Session 9: Keynote talk 2: **Monica Retamal** "Women's Digital Empowerment" (chairs: Paola Yang, Renata Mella)	
15:50-16:30	Session 10: WICAS Invited Talk: Moderator: Yoko Uwate, Sanjida Moury, "The Next-Generation Power Electronics Interface for Green Applications" (chairs: Renata Mella, Paola Yang)	
15:50-16:00	s1	Yoko Uwate. WiCAS Introduction
16:00-16:30	s2	Sanjida Moury. The Next-Generation Power Electronics Interface for Green Applications
16:30-17:30	Session 11: WICAS Panel: "Renewable Energy and Climate Change", Moderators: Renata Mella, Paola Yang, Panelists: Sanjida Moury, Claudia Rahmann, third TBD(chairs: Renata Mella, Paola Yang)	
Thursday, March 3rd		
08:45-10:00	Session 12: Keynote talk 3: **Boris Murmann** "Mixed-Signal Circuit Design for the Data-Driven World" (chair: Angel Abusleme)	
10:00-10:15	**Coffee Break**	
10:15-11:35	Session 13A: Parallel Th1A Nano-electronic Circuits and Systems II - Track 10 (chair: Maciej Ogorzalek)	
10:15-10:35	37	Gabriel Andrés Sanca, Fabrizio Di Francesco, Federico Golmar and Cynthia Paula Quinteros. Collective electrical response of simulated memristive arrays using SPICE
10:35-10:55	53	Theodoros Chatzinikolaou, Iosif-Angelos Fyrigos, Vasileios Ntinas, Stavros Kitsios, Panagiotis Bousoulas, Michail-Antisthenis Tsompanas, Dimitris Tsoukalas, Andrew Adamatzky and Georgios Ch. Sirakoulis. Memristor-based Oscillator for Complex Chemical Wave Logic Computations: Fredkin Gate Paradigm
10:55-11:15	8	Fernando José Costa, Renan Trevisoli Doria and Rodrigo Trevisoli Doria. SOI UTBB Capacitive Cross-Coupling Effects in Ultimate Technological Nodes
11:15-11:35	71	Laysson Luz, José Augusto Miranda Nacif, Ricardo Santos Ferreira and Omar Paranaíba Vilela Neto. An NML in-plane Wire Crossing Structure
10:15-11:35	Session 13B: Parallel Th1B Design Automation I -Track 4 (chair: Dinesh Bhatia)	

10:15-10:35	14	Vasileios Leon, Georgios Makris, Sotirios Xydis, Kiamal Pekmestzi and Dimitrios Soudris. MAx-DNN: Multi-Level Arithmetic Approximation for Energy-Efficient DNN Hardware Accelerators
10:35-10:55	26	Gabriel Duarte, Duarte Oliveira and Gracieth Batista. Design of Asynchronous Pipelines with QDI Template Using Commercial FPGA
10:55-11:15	36	Masoud Shahshahani and Dinesh Bhatia. PPA Based CNN Architecture Explorer
11:15-11:35	46	Henrique Kessler, Murilo Bohlke, Leomar da Rosa Jr., Marcelo Porto and Vinícius Camargo. Calibration of Logical Effort Transistor Sizing for On-the-Fly Low-Power Supergate Design
10:15-11:35	Session 13C: Iberchip I (chair: Fabián Olivera)	
10:15-10:35	110	Linton Esteves, Wagner Oliveira and Paulo Farias. Aceleração do cálculo do menor caminho em planejamento de rotas de robôs em tempo real
10:35-10:55	112	Clayton Farias, Paulo F. Butzen and Rafael B. Schvittz. Procedimento para estimativa da susceptibilidade à radiação de circuitos combinacionais
10:55-11:15	115	Matheus Pontes, Rafael Schvittz, Leomar S. Rosa Junior and Paulo F. Butzen. O Impacto da Susceptibilidade das Portas Lógicas na Estimativa da Confiabilidade de Circuitos
11:15-11:35	111	Nestor Pereira Neto, Wagner de Oliveira and Paulo Farias. Comunicação entre Robot Operating System - ROS e SoC com FPGA integrado
11:35-11:55	118	Gustavo Groeff, João Vitor Silveira and Calebe Conceicao. Adicionando à Qiskit suporte para simular algoritmos quânticos remotamente em FPGA
11:40-13:00	Session 14A: Parallel Th2A Sensors -Track 7	
11:40-12:00	28	Maximilian Scherzer, Mario Auer, Aris Valavanoglou and Werner Magnes. Implementation of a Fully Differential Low Noise Current Source for Fluxgate Sensors
12:00-12:20	5	Marco Antonio Menezes, Tales Pimenta and Carlos Martinez. Validation of an Signal Acquisition for Electrochemical Noise Corrosion Monitoring System
12:20-12:40	43	Minghao Li, Anne Vanhoestenberghe and Sara Ghoreishizadeh. An integrated circuit to enable electrodeposition and amperometric readout of sensing electrodes on-chip
12:40-13:00	64	Takuya Tsujimura. CMOS-Based Biosensor Using Broadband Tunable Active-Inductor-Based VCO with γ-Dispersion for Detecting CTCs and Exosomes
11:40-13:00	Session 14B: Parallel Th2B Digital Circuits and Systems I -Track 2	
11:40-12:00	55	Anagha Nimbekar, Y V Sai Dinesh, Arvind Gautum, Vidhumouli Hunsigida, Appa Rao Nali and Acharyya Amit. VLSI Architecture Design Methodology for Deep learning based Upper Limb and Lower Limb Movement Classification for Rehabilitation Application
12:00-12:20	39	Gundlapalle Vishnuvardhan and Acharyya Amit. A Novel Single Lead to 12-Lead ECG Reconstruction Methodology Using Convolutional Neural Networks and LSTM

12:20-12:40	60	Prasannata Bhange, Deepak Kumar Joshi Joshi, Acharyya Amit, Sunil Kumar Pandu, Kamal Mankari, Swati Ghosh Acharyya and Sridhar K. Phase Space Reconstruction Based Real Time Fatigue Crack Growth Estimation for Structural Health Monitoring Ships
12:40-13:00	23	Duarte Oliveira, Nicolly Cardoso and Gracieth Batista. Synthesis of QDI Combinational Circuits Implemented on Optimized Model
13:00-14:40	**Lunch**	
14:40-15:50	Session 15: Keynote talk 4: **Pierre-Emmanuel Gaillardon** "Under the Hood of OpenFPGA" (chair: Yann Deval)	
15:50-17:30	Session 16A: Parallel Th3A Analog and Mixed Signal Circuits and Systems I - Track 1	
15:50-16:10	6	Fabián Olivera, Lucas Souza da Silva and Antonio Petraglia. Ultra-Low-Power CMOS Voltage Reference Topologies Regarding Technology Node
16:10-16:30	22	David Palomeque-Mangut, Ángel Rodríguez-Vázquez and Manuel Delgado-Restituto. A Wide-Range, High-Voltage, Floating Level Shifter with Charge Refreshing in a Standard 180 nm CMOS Process
16:30-16:50	50	Xujiaming Chen, Guowei Chen, Xinyang Yu, Yue Wang and Kiichi Niitsu. A 52.3% Peak Efficiency 22nm CMOS Low-Power Light-Adaptive Self-Oscillating Voltage Doubler Using Scalable Dynamic Leakage-Suppression Logic
16:50-17:10	86	Pablo Pérez-Nicoli, Francisco Veirano and Fernando Silveira. A Compact Lithium-Ion Battery Charger for Low-Power Applications
17:10-17:30	88	Kato Sora, Chen Guowei and Niitsu Kiichi. A Ultra-Low Power 22nm Self-Oscillating Voltage Doubler With Dynamic Leakage-Suppression Logic
15:50-17:30	Session 16B: Parallel Th3B Digital Circuits and Systems II - Track 2	
15:50-16:10	54	Md Sazzad Hossain, Mateus Bernardino Moreira, Francois Sandrez, Francois Rivet, Herve Lapuyade and Yann Deval. Low Power Frequency Dividers using TSPC logic in 28nm FDSOI Technology
16:10-16:30	58	Huy Duong, Guowei Chen and Kiichi Niitsu. 22nm CMOS pW Standby Power Flip-Flops with/without Security using Dynamic Leakage Suppression Logic
16:30-16:50	70	Onur Karataş and Salih Ergün. A Digital Random Number Generator Based on Four Regional Examination of Double Scroll Chaos
16:50-17:10	99	Anudeep Bonasu, Aaron Stillmaker and Shahab Tayeb. Low-Power Vehicular Network ASIC Implementation
17:10-17:30	11	Palak Yash, Mansi Thakare and Babita Jajodia. Optimized Hardware Implementation of Vedic Binary Multiplier using Nikhilam Sutra on FPGA

15:50-17:30	Session 16C: Parallel Th3C SS2 - Application of Technology for Agrifood (chairs: Matias Miguez, Danilo Demarchi)	
15:50-16:10	109	Diego Barrettino. Sensor Systems for Smart Agriculture
16:10-16:30	66	Victor Grimblatt, Guillaume Ferré, Christophe Jego and Francois Rivet. An IoT SoC for Agricultural Applications
16:30-16:50	101	Enzo Pacilio, Alejo Silvarrey and Alvaro Pardo. UAVs vs Satellites: Comparison of tools for water quality monitoring V2
16:50-17:10	24	Mattia Barezzi, Umberto Garlando, Francesca Pettiti, Luca Nari, Davide Gisolo, Davide Canone and Danilo Demarchi. Long-Range Low-Power Soil Water Content Monitoring System for Precision Agriculture
17:10-17:30	82	Arnaud Alfredo, Matías Miguez, Juan Sapriza, Bruno Bellini and Felipe Estevez. Smart devices and RFID: towards an Android-based information system in the cattle-yards
17:45-19:15	Session 17: Panel "Heterogeneous 3D Integration" Moderator/Organizer Malgorzata Chrzanowska-Jeske, Panelists: Giovanni De Micheli, Pierre-Emmanuel Gaillardon, Maciej Ogorzalek, Ricardo Reis (chairs: Francois Rivet, Malgorzata Chrzanowska-Jeske)	
20:00-22:00	**Gala Dinner**	
Friday, March 4th		
08:45-10:00	Session 18: Keynote talk 5: Sorin Cotofana "Spin Wave Based Computing: Promises and Hurdles on the Road" (chair: Ricardo Reis)	
10:00-10:15	**Coffee Break**	
10:15-11:55	Session 19A: Parallel F1A Analog and Mixed Signal Circuits and Systems II-Track 1	
10:15-10:35	9	Bruno Canal, Hamilton Klimach, Sergio Bampi and Tiago Balen. Hybrid Comparator and Window Switching Scheme for low-power SAR ADC
10:35-10:55	32	Andrés Asprilla, Andreia Cathelin and Yann Deval. Highly Linear Large Signal Compact Voltage-to-Current Converter in 28 nm FD-SOI Technology
10:55-11:15	51	Renzo Barraza, Angel Abusleme and Sergey Kuleshov. TISIRC: A multichannel ASIC with gain control for SiPM detectors
11:15-11:35	65	Tatiana Moposita, Lionel Trojman, Marco Lanuzza, Felice Crupi and Andrei Vladimirescu. Voltage-to-Voltage Sigmoid Neuron Activation Function Design for Artificial Neural Networks
11:35-11:55	89	Kaya Demir and Salih Ergun. Random Number Generators Based on Metastable Behavior in Double-Scroll Chaotic Attractors
10:15-11:55	Session 19B: Parallel F1B Applied Circuits and Systems - Track 9 (chair: Malgorzata Chrzanowska-Jeske)	

10:15-10:35	38	Xiu Qi Chang, Ann Feng Chew, Benjamin Chen Ming Choong, Shuhui Wang, Rui Han, Rajesh C. Panicker and Deepu John. AFib Detection Using Weight-Pruned, Log-Quantised Convolutional Neural Networks
10:35-10:55	49	Xiaolin Li, Xiang Fang, Rajesh Panicker, Barry Cardiff and Deepu John. Classification of ECG based on Hybrid Features using CNNs for Wearable Applications
10:55-11:15	77	Francisco Veirano, Pablo Pérez-Nicoli, Nicolás Gammarano, German Fierro and Fernando Silveira. Near threshold pulse transit time processor for central blood pressure estimation
11:15-11:35	30	Muhammad Tanweer, Samu Järvinen and Kari Halonen. A low-noise analog front-end for wearablebiomedical devices featured with DRL and drivenconductor-shields
11:35-11:55	119	Rafael Medina, Joshua Klein, Yasir Qureshi, Marina Zapater, Giovanni Ansaloni and David Atienza. Full System Exploration of On-Chip Wireless Communication on Many-Core Architectures
10:15-11:35	Session 19C: Iberchip II (chair: Ramiro Taco)	
10:15-10:35	113	Humberto Matheus Costa Abádio, Fabián Olivera and Antonio Petraglia. Settling Time Modeling of the N-Stage Charge Pump Doubler Using Z Transform
10:35-10:55	114	Martina Rodrigues, Paulo César Aguirre, Alessandro Girardi and Natalia Chagas. A Low-Voltage R-2R DAC For Low Power Applications
10:55-11:15	116	FayÇal Haizouni, Kevin Vicuna and Ramiro Taco. Assesment and Optimization Variable Approximate Multipliers
11:15-11:35	117	Alesandro Bedoya, Cristhopher Mosquera and Ramiro Taco. Energy and Delay comparisons for XOR gates using Dual Mode Logic and Dual Mode Pass Logic
11:40-13:00	Session 20: Parallel F2B Development of high efficiency & HF circuits for power electronics converters - SS1 (chairs: Johan Guzman, Marcelo Perez)	
11:40-12:00	33	Guiyi Dong, Shogo Katayama, Yifei Sun, Yasunori Kobori, Anna Kuwana and Haruo Kobayashi. Notch Frequency Generation Methods in Noise Spread Spectrum for Pulse Coding Switching DC-DC Converter
12:00-12:20	103	Benjamin Coquillas, Eric Kerherve, Anne-Charlotte Amiaud, Laurent Roussel, Samuel Redois, Bruno Louis, Thomas Merlet and Vincent Petit. A Highly Compact 1W Ku-Band Power Amplifier
12:20-12:40	102	Johan Guzman, Roberto Ramirez, Claudio Tenreiro, Sergio Diaz and Oscar Hernandez. A Low-Cost Cold Plasma Generator Circuits Designed for Laboratory Applications.
12:00-13:00	Session 21: Parallel F2A Design Automation II -Track 4 (chair: Maciej Ogorzalek)	
12:00-12:20	27	Pingakshaya Goswami, Masoud Shahshahani and Dinesh Bhatia. MLSBench: A Benchmark Set for Machine Learning based FPGA HLS Design Flows

12:20-12:40	75	Lucas Ribeiro, Ricardo Jacobi, Jones da Silva, Ivan Silva and Francisco Silva. Evaluating a Machine Learning-based Approach for Cache Configuration
12:40-13:00	40	Shoya Sonoda, Jun Shiomi and Hidetoshi Onodera. Approximation-Based Implementation for a Minimum Energy Point Tracking Algorithm over a Wide Operating Performance Region
13:00-14:40	**Lunch**	
14:40-15:50	Session 22: Embedded Tutorial: Maciej Ogorzalek "Towards New Architectures for 3D Integration" (chair: Ricardo Reis)	
15:50-16:50	**Closing Ceremony** (chairs: Victor Grimblatt, Yann Deval)	