Title: Power Analysis in VLSI Circuit Design: An Overview

Abstract

The semiconductor industry demands today low consumption products due to the constant development of mobile technology and high-performance computing. EDA (Electronic Design Automation) tools that optimize power consumption requires an appropriate power analysis to guide power optimization techniques correctly. This tutorial is an overview of power analysis applied to EDA tools with emphasis on the trade-off among accuracy, computing resources and time. The first part consists in a review of fundamental elements in modeling and characterization of power, i.e., how to move from SPICE to Liberty. Understanding digital circuits work under a context of activity, the second part applies the previous concepts discussed to power calculation and includes switching activity file generation. Finally, a discussion of power analysis applied to EDA tools and power optimizations is presented, including challenges and limitations.

Keywords: Power Characterization, Switching Activity, SAIF, EDA.

Learning Objectives

At the end of the tutorial presentation, the attendants will be able to:

- Recognize the importance of power analysis in the digital integrated circuits design
- Identify the main electronic components that affect power measurements.
- Understand the limitations of power modeling in EDA tools.
- Apply the fundamental concepts of power analysis to evaluate power optimization technique results.

Target Audience

The target audience of this tutorial are:

- Application engineers or developers working with EDA tool for VLSI or FPGA circuits
- Newcomers interested in becoming familiar with the power measurement methodologies used in EDA tools.
- Electrical and Computer Engineering graduate and undergraduate students interested in VLSI circuit designs.

Content

- Power Modeling and Characterization (1 Hour)
    - Switching Activity
    - Leakage, Internal, Switching
    - Liberty
- Power Calculation (1 Hour)
    - Leakage, Internal, Switching
    - Switching Activity and Accuracy
- Power Analysis in EDA tools (1 Hour)
    - Challenges and limitations

- Reports
- Power Optimizations

Speaker Biography

Joaquin A. Venegas Jara was born in Linares, Chile. He received the B.Sc. and M.Sc in electrical engineering from Pontifical Catholic University of Chile, Santiago, Chile in 2015. From 2015 to 2016, he worked as a R&D Engineer in the Verilog implementation of a multi-antenna wireless communication modem for a university research project. From 2016 to 2017, Joaquin oversaw the development and manufacture of meteorological stations based on wireless sensor networks in a startup, Refine. He has been an instructor of the Digital Integrated Circuit Design course at Pontifical Catholic University of Chile from 2018 to 2021. Since 2019, he is a product application engineer in Synopsys for the area of power analysis and clock gating.

His interests include power analysis in VLSI designs, wireless sensor networks, Internet of Things applications and data visualization.