Improving integrated circuit reliability by combining tests to ionizing radiation and electromagnetic compatibility

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Presenter

Abstract:
Technology scaling, which made electronics accessible and affordable for almost everyone on the globe, has advanced IC and electronics since sixties. Nevertheless, it is well recognized that such scaling has introduced new (and major) reliability challenges to the semiconductor industry. This tutorial addresses the background mechanisms impacting reliability of very deep submicron (VDSM) integrated circuits (ICs). In more detail, topics such as the basics about electromagnetic compatibility (EMC) and ionizing radiation, the mechanisms by which they affect ICs, the current standards and laboratory test infrastructure for EMC, total-ionizing dose (TID) and single-event effects (SEEs) on ICs are presented and their combined effects on the reliability of modern ICs are discussed. Moreover, the way reliability failure mechanisms for (ionizing and non-ionizing) radiation are modeled and how they are impacting IC aging and lifetime will be covered. Recent results from laboratory experimental measurements are described. Classic design solutions to counteract with TID, SEEs, aging and EMC in VDSM ICs as well as the recent achievements on the development of on-chip sensors to monitor EM conducted noise on IC power supply lines are introduced. A YouTube video is presented to illustrate the effectiveness of such on-chip sensors to detect aging. Finally, Spice simulations are used to demonstrate the combined effect of ionizing radiation with power supply noise on SRAM cells followed by the presentation of some measures to counteract with it.

Duration of the Tutorial: ~60 minutes.

Target Audience: IC- and system-level designers (engineers and PhD students) working on aerospace, defense & security applications.

Authors' Short Bios:

Fabian Vargas obtained his Ph.D. Degree in Microelectronics from the Institut National Polytechnique de Grenoble (INPG), France, in 1995. At present, he is Full Professor at the Catholic University (PUCRS) in Porto Alegre, Brazil. His main research domains involve the HW-SW co-design and test of system-on-chip (SoC) for critical applications, system-level design methodologies for radiation, accelerated aging and electromagnetic compatibility, embedded sensor design for characterization, reliability and aging binning. Among several activities, Prof. Vargas has served as Technical Committee Member or Guest-Editor in many IEEE-sponsored conferences and journals. He holds 9 BR and international patents, co-authored a book and published over 200 refereed papers. Prof. Vargas is associate researcher of the BR National Science Foundation since 1996.

He co-founded the IEEE-Computer Society Latin American Test Technology Technical Council (LA-TTTC) in 1997 and the IEEE Latin American Test Symposium - LATS (former Latin American Test Workshop - LATW) in 2000. Prof. Vargas received for several times the Meritorious Service Award of the IEEE Computer Society for providing significant services as chair of the IEEE Latin American Regional TTTC Group and the LATS. Prof. Vargas is a Golden Core Member of the IEEE Computer Society and Senior Member of the IEEE.

Bernd Deutschmann is Full Professor for Electronics and head of the Institute of Electronics at Graz University of Technology/Austria. He received his M.Sc. degree and the Ph.D. degree in telecommunication engineering from the Graz University of Technology in 1999 and 2002, respectively. From 2000 to 2006 he was with austriamicrosystems AG/Austria working on the improvement of the electromagnetic compatibility (EMC) of integrated circuits. In 2006, he joined Infineon Technologies AG in Munich/Germany, where he focused his research activities on EMC aware IC design and EMC simulation of ICs for automotive power applications. In 2014 he returned to academia and joined Graz University of Technology as a Full Professor. His research area is the design of electronic systems and integrated circuits with a special focus on their electromagnetic compatibility. This area covers topics as reduction of the electromagnetic emission, improvement of the immunity against transient disturbances and radio frequency interferences, EMC simulation, EMI propagation in integrated circuits, EMC characterization of integrated circuits, and susceptibility of analog building blocks. During his research activities, he has applied for several patents and has authored and coauthored numerous papers and technical articles in the field of electromagnetic compatibility of integrated circuits.

Sonia Ben Dhia is Full Professor at INSA-Toulouse (French engineering institute) since 2000, Department of Electrical and Computer Engineering, she teaches digital electronics, IC testability and reliability, and analog and RF CMOS design. As CEO of INSA Euro-Méditerranée, Fès, Morocco (2014-2017), she was responsible for the overall leadership and management of this new engineering institute. This included courses and curriculum development, students' recruitment, staff and students' development, research leadership as well as national and international professional and academic linkages.

Her research interests at LAAS – CNRS Toulouse include signal integrity in nano-scale CMOS ICs, electromagnetic compatibility and reliability of ICs. She has authored and co-authored 3 books, more than 100 publications in peer-reviewed journals & conference proceedings and supervised 13 PhD theses and 8 M.Sc. theses. For further information, please address http://gei.insa-toulouse.fr/fr/departement/people/sonia-ben-dhia.html.