

Proposal for Tutorial

Title: Taking ownership of your Physical Design Kits

Length: 3 Hours

Abstract:

Interoperable Physical Design Kits (iPDKs) have become essential to modern IC design flows. This tutorial will discuss the anatomy of an iPDK. These packages, which can be managed across tools of different vendors and purposes, are typically composed of simulation models, extraction and manufacturing rules, automatic layout cells and other files. We will go into details of how these files are used, how these are packed together and how they interact with different tools. This information will be leveraged later as we walk you through an example on how to develop Python based PCells (PyCells) that can be used to increase productivity of implementation of custom analog, digital and mixed signal circuits. PCells are parametrized cells which can implement semi-automated layout generation of devices using technology information.

Keywords: PDK, iPDK, EDA, PCells, PyCells. CDF.

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Learning Objectives:

- Introduce the audience the concept of interoperable PDK
- Understand the contents of a PDK and how the files are used during flow
- Understand the development flow of PyCells for custom devices

Target Audience:

- Engineers or Students with background on IC Design
- CAD Engineers looking for a better understanding of implementation tools
- IC Designers who want to customize their vendor provided libraries

Full Description (Tentative Outline):

- I. Introduction
 - A. What is, what it is used for and who build them
 - B. Applications that consume them
 - C. Concept of Interoperability and the contents of an iPDK
- II. PDK Infrastructure
 - A. Anatomy and organization
 - B. Technology file / Display files / Scripts / Documents
 - C. Open Access
- III. Front End - Schematic Design
 - A. Devices Symbols
 - B. Device Parameters and iCDFs
 - C. SimInfo / Netlister / Simulation Views
 - D. Callbacks

- IV. Back End - Layout Design**
 - A. PyCell Development Flow**
 - B. Advanced PyCell features**
 - C. SDL**
 - D. Physical Verification & Extraction**
 - E. Post Layout Simulations**