Tutorial: *Soft and Permanent Errors in Digital Cameras: Analysis, Detection, and Tolerance*

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The CMOS Active Pixel Sensor (APS) in current digital cameras, like any other digital circuit, is subject to both soft and permanent faults. However, the manifestation of such faults and the available techniques for detecting them and for tolerating them are very different. This tutorial summarizes the experimental and theoretical research results that we have obtained in our ongoing research of digital sensors' defects for the last 15 years.

We start by identifying the unique type of permanent faults that occur in digital cameras' sensors. We then analyze their behavior and identify their possible source. We describe an algorithm capable of detecting these faults during the normal operation of the camera. Such an online detection allows us to develop efficient techniques for greatly reducing their impact on the quality of the image without having them undergo an in-factory re-calibration.

We next focus on soft errors (also known in the literature as Single Event Upsets - SEUs) that are typically caused by hits of high-energy cosmic particles. In regular digital circuits, if the charge deposited by a particle hit is too small to change the state of a flip-flop, there will be no indication that such a hit ever occurred. In contrast to other ICs, the CMOS APS in a digital camera can record the effect of most particle hits by displaying a pixel output that is brighter than the incoming illumination. We present an experimental study of SEUs in digital cameras and compare their rate to that of SEUs in SRAM memory and to the rate of permanent defects in cameras. This analysis provides important information about the nature and distribution of particle hits and their occurrence rate, and increases our understanding of SEUs in regular ICs as well as in camera sensors.

Area of tutorial: *Fault-tolerant circuits and Circuit testing.*

Learning Objectives: *Understand the source and distribution of soft and permanent faults in imagers, study techniques to detect faults during on-line operation to reduce their impact, understand the nature and distribution of particle hits causing SEUs in imagers and regular ICs.*

Target audience and prerequisites: *Researchers and practitioners of testing techniques and fault tolerant circuits.*

Biographical Data

NAME: ISRAEL KOREN

ACADEMIC RANK: Professor

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EDUCATION: B.Sc., M.Sc., Ph.D., Electrical Engineering, Technion - Israel Institute of Technology, 1967, 1970, 1975

ACADEMIC POSITIONS:

1987 to present	Professor, Electrical & Computer Eng., University of Mass, Amherst
1985 to 1986	Head, VLSI Systems Research Center, Technion, Haifa, Israel
1982 to 1983	Visiting professor at the University of California at Berkeley, CA
1979 to 1985	Senior Lecturer, Department of Electrical Engineering, Technion, Israel
1978 to 1979	Assistant Professor, University of Southern California, Los Angeles, CA
1976 to 1978	Assistant Professor, University of California, Santa Barbara, CA

CONSULTING:

Consultant to AMD, Analog Devices, BlueRisc, Digital Equipment Corporation, ELTA, IBM, Intel Corporation, National Semiconductor, Tolerant Systems, and Tadiran.
Member of the Advisory Board: Ponte Solutions, Adapteva.

PATENTS:

1. US Patent 7,278,136: Reducing processor energy consumption using compile-time information, Oct. 2007.
2. US Patent 6,934,865: Controlling a processor resource based on a compile-time prediction of number of instructions-per-cycle that will be executed across plural cycles by the processor, Aug. 2005.
3. US Patent 7,408,578: Active pixel with built in self-repair and redundancy, Aug. 2008.

PUBLICATIONS RELEVANT TO THE TUTORIAL:

- Textbook: Computer Arithmetic Algorithms, 2nd Edition, A.K. Peters, MA, 2002.
- Textbook: Fault Tolerant Systems, I. Koren and C. M. Krishna, Morgan-Kaufman Publishers, March 2007.
- J. Dudas, L.M. Wu, C. Jung, G.H. Chapman, Z. Koren, and I. Koren, "Identification of in-field defect development in digital image sensors," *Proc. Electronic Imaging, Digital Photography III*, v6502, 65020Y1-0Y12, San Jose, Jan 2007.
- J. Leung, G. Chapman, I. Koren, and Z. Koren, "Automatic Detection of In-field Defect Growth in Image Sensors," *Proc. of the 2008 IEEE Intern. Symposium on Defect and Fault Tolerance in VLSI Systems*, 220-228, Boston, MA, Oct. 2008.
- J. Leung, G.H. Chapman, I. Koren, and Z. Koren, "Statistical Identification and Analysis of Defect Development in Digital Imagers," *Proc. SPIE Electronic Imaging, Digital Photography V*, v7250, 742903-1 – 03-12, San Jose, Jan 2009.

- J. Leung, G. H. Chapman, I. Koren, Z. Koren, "Tradeoffs in imager design with respect to pixel defect rates," *Proc. of the 2010 Intern. Symposium on Defect and Fault Tolerance in VLSI*, 231-239., Kyoto, Japan, Oct 2010.
- J. Leung, G.H. Chapman, Y.H. Choi, R. Thomson, I. Koren, and Z. Koren, "Tradeoffs in imager design parameters for sensor reliability," Proc*., Electronic Imaging, Sensors, Cameras, and Systems for Industrial/Scientific Applications XI*, v 7875, 78750I1-0I12, San Jose, Jan. 2011.
- G.H. Chapman, I. Koren and Z. Koren, "Do More Camera Pixels Result in a Better Picture?" *Proc. IEEE 18th International On-Line Testing Symposium (IOLTS),* pp. 75-78, June 2012.
- G.H. Chapman, R. Thomas, I. Koren, and Z. Koren, "Empirical formula for rates of hot pixel defects based on pixel size, sensor area and ISO", *Proc. Electronic Imaging, Sensors, Cameras, and Systems for Industrial/Scientific Applications XIII*, v8659, 2013.
- G.H. Chapman, R. Thomas, R. Thomas, K. Meneses, T. Yang, I. Koren, and Z. Koren, "Single Event Upsets and Hot Pixels in Digital Imagers," *Proc. 2015 Intern. Symposium on Defect and Fault Tolerance in VLSI*, pp. 41-46, Oct. 2015.
- G.H. Chapman, R. Thomas, R. Thomas, I. Koren, and Z. Koren, "Experimental Study and Analysis of Soft and Permanent Errors in Digital Cameras," *Proc. 2016 Intern. Symposium on Defect and Fault Tolerance in VLSI*, pp. 41-46, Oct. 2016.

HONORS AND AWARDS: IEEE Fellow, Fellow of Japan Society for the Promotion of Science

INSTITUTIONAL AND PROFESSIONAL SERVICE IN THE LAST 5 YEARS:

1. Highlight presentation, "Exploring Heterogeneity within a Core for Improved Power Efficiency," 8th ACM International Systems and Storage Conference (SYSTOR'15), May 2015.
2. General chair - *The 25th IEEE Symposium on Computer Arithmetic*, June 2018.
3. Keynote Address, "Yield Modeling: Theory and Practice," 2012 IEEE Intern. Symp. on Defect and Fault Tolerance in VLSI & Nanotechnology Systems, Oct. 2012.
4. Associate editor of Sustainable Computing: Informatics and Systems since 2010.
5. Associate editor of VLSI Design Journal, 2006-2015.
6. Guest Editor (with D. Mosse) of a Special Issue of the Sustainable Computing: Informatics and Systems Journal on the IEEE Green Computing Conference (IGCC 2011), July 2012.
7. Program Committee member - 43rd IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), June 2013.
8. Program Committee member - ACM 2013-2015 Research in Adaptive and Convergent Systems (RACS 2013-2015), October 2013, 2014 and 2015.
9. Program Committee member - IEEE Workshop on Dependable Many-Core Computing (DMCC 2012-2013), July 2012, July 2013.
10. Editorial Board member - book series "Sustainable Energy Developments," CRC Press.
11. Steering Committee member - IGCC - International Green Computing Conference.
12. Steering Committee member - ARITH - International IEEE Computer Arithmetic Symposium.
13. Co-General Chair, FDTC 2004-2016 - Fault Diagnosis & Tolerance in Cryptography.
14. Co-General Chair, the 2013-2015 Workshops on Cryptography and Security in Computing Systems.
15. Program Committee member - 4th IEEE International Conference on Sustainable Computing and Communication, Dec. 2014.
16. Program Committee member - HotChips 2013.
17. Program Committee member - 3rd and 4th Workshops on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'14 and '15), March 2014 and Nov. 2015.
18. Program Committee member - IGCC 2013 - International Green Computing Conference, June 2013.