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Tutorial Proposal

Why FinFETs, Why 3D ICs - are we ready for technology revolution?

Half-day ~ 3 hours

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Area: VLSI Systems and Applications

Abstract:

We begin with a discussion of the limitations of the most common silicon-based CMOS Technologies. This first part of the tutorial tries to give answers to two questions: Why FinFETS and why 3D integration? As the sizing of the transistors comes to the atomic distance limitations further development becomes possible by extending the channels and gates of the transistors into 3D exploiting various 3D geometries such as for example FinFETS or 3D nanowire transistors NWMOS.

Limitations in microcircuit constructions can be avoided by 3D integration that offers unprecedented opportunities by allowing blocks fabricated in heterogeneous technologies to be integrated in one chip. Such an approach allows for efficient space usage at the same time allowing circuit footprint reduction and offers very significant wirelength reductions thus reducing power dissipations and signal delays.

The second part focuses on physical properties of 3D integrations such as thermal issues, interconnect density, and their influence on operation and performance optimization of 3D ICs integrated vertically using through silicon vias (TSVs). The most significant challenge for continued integration of complex systems is energy efficiency, and 3D heterogeneous stacking of diverse circuit blocks is one of the most promising solutions.

Many of the advantages strongly depend on 3D layout that defines interconnect length and densities, and power distribution on individual device layers. The importance of accurate analysis and optimization during 3D floorplanning is discussed. In comparison to 2D, 3D ICs have smaller footprint area and therefore smaller heat sink area, which leads to heat accumulation. Without effective cooling mechanisms and clear understanding of their impact on 3D ICs the thermal degradation could overshadow advantages of 3D integration.

We also look towards new incoming technologies like monolithic 3D systems, new materials such as carbon-nanotubes, and energy and heat-removal efficient interconnects. The question of if we are ready for technology revolution will be addressed.

Keywords: 3D ICs, TSV Technology and Modeling, Energy Efficiency, Performance, System Optimization, hybrid systems, emerging technologies

Speakers' Bios

Maciej Ogorzałek is professor of Electrical Engineering and Computer Science and head of the Department of Information Technologies, Jagiellonian University (the oldest academic institution in Poland, founded in 1364) in Krakow, Poland. He held several visiting positions in Denmark, Switzerland, Germany, Spain, Japan, and Hong Kong. Dr. Ogorzalek received a Research Award from the Ministry of Education of Spain in 2000 and worked for one year at the National Microelectronic Center, Seville, Spain. In 2001 he received a Senior Award from the Japan Society for Promotion of Science as visiting professor at Kyoto University and in 2005 a Hertie Foundation Fellowship at the Goethe University Frankfurt-am-Main. From 2006–2009 he held the chair of Biosignals and Systems, Hong Kong Polytechnic University, under the Distinguished Scholars Scheme. His research interests include nonlinear systems, chaos and complexity, bio-medical signal and image processing, new approaches to design of 3D microelectronic circuits, applications of computational intelligence techniques in system design, and signal/image analysis and classification. Dr. Ogorzalek is author or co-author of over 280 technical papers published in journals and conference proceedings, and author of the book Chaos and Complexity in Nonlinear Electronic Circuits (World Scientific, 1997). He served as executive vice-president of the Sniadecki Science Foundation (until 2006).

He served as editor-in-chief of the Circuits and Systems Magazine (2004–2007), associate editor of Proceedings of the IEEE (2004–2009), associate editor for the IEEE Transactions on Circuits and Systems Part I (1993–1995 and 1999–2001). He also serves as an associate editor of International Journal of Bifurcations and Chaos (2004–), Journal of the Franklin Institute (1997–), secretary of the editorial board for the Quarterly of Electrical Engineering (1993–2000), member of the editorial board of Automatics (in Polish), and member of the editorial board of the International Journal of Circuit Theory and Applications (in Polish) (2000–). Since 2009 he is an associate editor of the NOLTA Journal (Japan).

Dr. Ogorzalek is an IEEE fellow (1997). He served the IEEE Circuits and Systems Society in various capacities including the Society president in 2008. He presented numerous keynote, plenary and tutorial lectures at conferences world-wide (total 53!). He was CAS Society Distinguished Lecturer (2004–2005) and received the 2002 Guillemin-Cauer Award and IEEE-CAS Golden Jubilee Award. In 2012 he has been elected member of the Academia Europaea. In 2016-2017 he serves as an elected member of the IEEE Board of Directors - Division 1 Director.

Malgorzata Chrzanowska-Jeske is Professor of Electrical and Computer Engineering and Director of the VLSI & Emerging Technology Design Automation Laboratory at Portland State University. From 2004 to 2010 she was Chair of the ECE department at PSU, which she joined in 1989. Previously, she has served on the faculty of the Technical University of Warsaw, and as a design automation specialist at the Research and Production Center of Semiconductor Devices in Warsaw. She holds M.S. degree in electronics engineering from Politechnika Warszawska (the Technical University of Warsaw) Warsaw, Poland, and the PhD degree in electrical engineering from Auburn University, Auburn, Alabama.

Her research interests include CAD for VLSI ICs, MS-SOCs, 3D ICs, nanotechnology and nano/bio systems, design for manufacturability and design issues in emerging and renewable technologies. She has presented tutorials, keynote and invited talks at various international conferences and events. She has published more than 150 technical papers and serves as a panelist and reviewer for the National Science Foundation (NSF), and as a reviewer for National Research Council Canada (NRC) and many international journals and conferences. Her research has been supported by the NSF and industry.

Dr. Chrzanowska-Jeske has served in various roles on the Technical, Steering, and Organizing Committees of many international conferences and workshops, and as Senior Editor, Associate Editor and Guest Editor of international journals. Currently, she serves as Associate Editor for Transactions on Circuits and Systems II. She served for two terms on Board of Governors of IEEE Circuits and Systems Society (CASS) where she was also Chair of the Distinguished Lecturer Program and Chair and a founding-member of Women in CAS. Currently, she serves as Vice President for Technical Activities for the IEEE Nanotechnology Council (NTC), and is chair elect of Nanoelectronics and Giga-scale Systems Technical Committee of the IEEE Circuits and Systems Society. She presented keynote, plenary and tutorial lectures at various international conferences. She received the Best Paper Award from Alabama Section of IEEE for the best IEEE Transaction paper in 1990 and IEEE Council on Electronic Design Automation 2008 Donald O. Pederson Best Paper Award in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems.

Previous Offerings: Part of an older and differently focused version was offered at LASCAS 2013, and ISCAS 2014.

Learning Objectives: Current CMOS devices and IC microarchitecture limitations. Possible solutions by moving into 3D for devices (FINFETs, NWMOS) and for architecture (3D ICs). Integration of heterogeneous technologies. Current state-of-the-art technology for 3D ICs with through silicon vias. Discuss main challenges and possible advantages. New trend in device structures and system architecture.

Target audience: Electrical engineers with basic understanding of digital circuit design and its challenges due to scaling. Attendees with experience in digital circuit design and those

interested in energy efficient design options will appreciate this comprehensive presentation on TSV-based 3D stacking.

Tutorial description:

We begin this tutorial with a discussion of the limitations of the most common silicon-based CMOS Technologies. Two possible ways of further development are considered – named respectively "more Moore" and "more then Moore" – referring to the famous predictions of developments of Technologies due to the founder of Intel, Gordon Moore. This first part of the tutorial tries to give answers to two questions: Why FinFETS and why 3D integration?

As the sizing of the transistors comes to the atomic distance limitations further development becomes possible by extending the channels and gates of the transistors into 3D exploiting various 3D geometries such as for example FinFETS or 3D nanowire transistors NWMOS.

Limitations in microcircuit constructions can be avoided by putting whole building blocks and sub-circuits in stacks. Such an approach allows for efficient space usage at the same time allowing circuit footprint reduction. Also routing solutions offer very significant wirelength reductions thus reducing power dissipations and signal delays. 3D integration looks as a fantastic new area of development, however, there are many new challenges and problems to be solved.

3D integration offers also unprecedented opportunities by allowing blocks fabricated in heterogeneous technologies to be integrated in one chip. This allows for stacking and integration of microprocessors, memories, RF circuitry, sensors, batteries and hyper-capacitors, energy harvesting blocks, biological and chemical sensors and many new types of building blocks in one chip.

The second part of the tutorial will focus on physical properties of 3D integrations such as thermal issues, interconnect density, and their influence on operation and performance optimization of three-dimensional integrated circuits (3D ICs) consisting of multiple layers of systems integrated vertically using through silicon vias (TSVs).

The most significant challenge for continued integration of complex systems is energy efficiency. 3D heterogeneous stacking of diverse circuit blocks is one of the most promising solutions. Advantages of 3D integration also include; short interconnect length, high packing density, high speed operation, improved band width, and effective integration of heterogeneous technologies.

Many of 3D integration advantages strongly depend on 3D layouts of these systems, and especially on three-dimensional floorplann that defines interconnect densities on individual device layers. In this tutorial we will focus on influence of wire congestion, thermal and coupling noise distributions on performance and power efficiency of homo- and heterogeneous complex systems. We will show the importance of accurate and careful analysis and optimization during 3D floorplanning. In comparison to 2D, 3D ICs have smaller footprint area and therefore smaller heat sink area that leads to heat accumulation. Without effective cooling mechanisms and clear understanding of their impact on 3D IC performance and power efficiency the thermal degradation of the 3D systems could overshadow advantages of 3D integration. Thermal crosstalk within heterogeneous 3D systems can elevate temperature for low-power dice and overall performance can be negatively affected. It is clear that the cost-effective design of 3D ICs will require fast and accurate new optimization approaches and tolls.

Challenging and non-trivial research questions resulting from these diverse dependencies will be addressed. We will also look towards new incoming technologies like monolithic 3D systems, new materials such as carbon-nanotubes, and energy and heat-removal efficient interconnects. The question of if we are ready for technology revolution will be addressed.