SRAM Design in Advanced Technology

Abstract of Tutorial: All SOCs have embedded SRAM to store data. As the processing power of a SOC increases, so is the demand for embedded SRAM. This makes SRAM a significant contributor to chip power, performance, area, and yield. In the first part of this tutorial we will start with the basics of SRAM design, and the basic feature set of an embedded SRAM. As SRAM is the primary contributor to overall chip yield, we will talk about different testability and yield enhancement techniques for SRAM arrays. As the power consumption of an SRAM array is a significant part of overall chip power, SRAM has different power management features, which we will also touch on. We will also discuss critical timings associated with SRAM.

In the second part of the tutorial we will discuss variability in SRAM and its implications. As CMOS technology scales, the density of the embedded memory in a chip increases. To reduce SOC size, the technological feature for SRAM is smaller than the logic transistor. The small size increases the susceptibility of variation in SRAM cell transistors. To reduce power consumption lower voltage is used, and the lower supply voltage along with variation causes SRAM cell writeability and cell stability issues. In the FINFET process the width of a transistor can only be based on the number of FINS. This makes SRAM design even more challenging. Due to the discrete nature of the width of the transistor, choices for transistor sizes are limited. Limitation on transistor sizes means SRAM cell issues cannot be addressed by process technology. To overcome this process challenge, transistors of 6T SRAM cells are dynamically made stronger and weaker by changing the bias conditions of transistors for different operations. Circuit used for dynamically changing strength of different transistor in a SRAM cell is called assist circuits. We will be talking about different assist techniques for embedded SRAM.

Area of Tutorial: Analog and Digital Circuit, Mixed mode circuits, SRAM design

Keywords: Semiconductor Memories, Static memories (SRAM), FINFET, 16nm, advanced technologies, memory technologies, Write Assist, Read disturb

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Learning Objectives:

To understand the basic features of embedded SRAM design, the different power management techniques in SRAM design, and understand what different timings associated with an embedded SRAM are. To learn how to make a robust memory with process variation, to understand the implication of advanced FINFET technology on SRAM design, and to understand the concept of writeability and access disturb. Finally, to learn about different design solutions for writeability and access disturb issues.

Target audience

SRAM researchers and designers, digital electronics researchers, and students

Prerequisite knowledge of audience:

Understanding of basic digital gates

Understanding of CMOS Transistors

Full Description:

In this tutorial we will cover SRAM design from the basics to practical issues in advanced technologies

1. **SRAM as an embedded memory**

   Due to its simple structure, fabrication process, and high density, SRAM technology has been the preferred choice of embedded memory for a long time. In this tutorial we will cover the following topics for SRAM design:

   - Basic 6T SRAM design
   - Standard feature of embedded SRAM
     - Write Mask
     - BIST Muxes
     - Write Through
     - Pseudo Scan
     - Soft Error Repair
   - Yield and test features for embedded SRAM
     - Aging Effect Nobs
     - Redundancy
     - Extra Margin Adjustment
     - Write Extra Margin Adjustment
   - Power management feature of embedded SRAM
     - Flex Banking
     - Level Shifting
     - Split Power Rail
     - Selective Precharge
     - Integrated Power Gates
     - Retention
     - External Power Gating
     - Left-right Bank Mask

2. **Timings in Embedded SRAM Arrays**

   - Cycle time: Cycle time is the maximum frequency at which an embedded memory can operate

   - Access time: During the read cycle, the time between when the edge of the clock rises until when data is received at the output bus is called access time.

   - Setup/hold time of input pin: All the synchronous input pins should maintain their setup and hold times with respect to the clock.

3. **Margining of Embedded SRAM Arrays**

   Embedded memory has to work with global as well as local variation with a range of supply voltages and temperatures. Functionality of embedded SRAM is ensured at extreme conditions, which is known as margining.

4. **FINFET based SRAM**

   In FINFET based SRAM, transistor sizes are multiples of the number of fins, which makes SRAM cell design challenging.

5. **Write-ability Issue in SRAM Cells**

   At low voltage, even if the bitline has been pulled low by the write driver, due to process variation the cell may have difficulty writing new data. This is known as writeability issue in SRAM.

6. **Access Disturb Issue in SRAM Cells**

   At low voltage, when we read or write SRAM, read operations can cause unintended write operations for all the cells in the row. During write operations half of the selected cells may have unintended write operations. This is known as access disturb.

7. **Different Methods for Increasing Writeability of SRAM Cells**

   a. Supply variation based methods: supply lowering can help increase writeability of cell.

   b. Bitline biasing based methods: Bringing the bitline to negative improves writeability of cell.

   c. Wordline biasing based methods: Boosting the word line to a higher voltage helps in write.

8. **Different Methods for Mitigating Disturb during Reading Data from an SRAM**

   a. Bitline biasing based methods: Lower bitline pre-charge helps in mitigating disturb.

   b. Wordline biasing based methods: Lowering wordline voltage reduces charge sharing and hence reduces disturbs.

   c. Supply biasing based methods: Increasing supply voltage or decreasing ground helps in reducing or eliminating cell disturb.

9. **Open Question and Answers**