Memristor Device Modeling and Applications in Memory, Logic, Computing and Learning

Area: Nanoelectronics

Abstract

The first physical realization of the Chua's memristor by the Hewlett-Packard Laboratories in 2008 created new tracks and trends in circuit design. The memristor, a nanoscale, nonvolatile, two-terminal resistive device whose resistance changes depending on the input signal applied to its terminals, is currently being explored for several emerging applications regarding upgraded and novel, energy-efficient digital/analog implementations such as nonlinear (chaotic) circuits, storage systems, logic circuits, neuromorphic and generally unconventional circuit architectures. This tutorial particularly considers the design, simulation and development of nanoelectronic circuits, systems and computing architectures focusing on memristor as the main storage and computing element. The ultimate goal is to explore and report the major related challenges and present state-of-the-art solutions for the smooth transition from conventional circuit technologies to emerging, beyond von Neumann computing nanotechnologies. The presented material spans from fundamental device modeling and emulating strategies, to emerging, dense, multi-level storage system architectures and novel, unconventional circuit design methodologies, targeting advanced analog/digital, massively parallel, neural-based computational structures. Fundamental details along with latest research results on memristor modeling, functionally-complete logic gates, multi-level nanocrossbar memory and applications of memristors in unconventional computing and learning, are presented. High-density memristive data storage combined with novel memristive circuit-design paradigms and computational tools able to solve NP-hard artificial intelligence problems, as well as memristor-based adaptive and learning units, certainly pave the way for a very promising memristive era in electronic systems and architectures where memory and processing co-exist. The discussed graph-based NP-hard problems are solved on memristive networks coupled with Cellular Automata (CA)-inspired parallel computational schemes. This tutorial covers a timely topic of academic and industrial interest and it may constitute an informative cornerstone for young scientists and a comprehensive reference to the experienced circuit designer and modeler, hoping to stimulate further research on memristive devices, circuits, and systems.

Keywords

memristor, resistive switching, memristor modeling, memristor emulator, emerging technologies, nanoelectronics, resistive RAM, unconventional computing, neuromorphic, neural network, artificial intelligence, learning.

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Dr. Ioannis Vourkas (S´12-M´16) was born in Kozani, Greece, in 1985. He received the M.Eng. (Diploma) and Ph.D. degrees, both in Electrical and Computer Engineering (ECE), from the Democritus University of Thrace (DUTh), Xanthi, Greece, in 2008 and 2014, respectively. In 2015 he was engaged in postdoctoral activities in the ECE Department of DUTh. Currently he is Postdoctoral Researcher with the Centro de Investigación en Nanotecnología y Materiales Avanzados (CIEN-UC), Department of Electrical Engineering, Pontificia Universidad Católica de Chile (PUC), Santiago, Chile.

In 2006 he received an annual performance award from the Greek State Scholarships Foundation (IKY) for completing the third year of his undergraduate studies rated first among all course students. Part of his Diploma Thesis was published in the DSP 2009 Conference, in Santorini, Greece, on 5-7 July, 2009. During his Ph.D. studies he focused on a highly interdisciplinary scientific area related to nanoelectronic circuits and systems based on resistive-switching devices (memristors). This research topic was found timely and important by the Greek Bodossaki Foundation which provided him with a full Ph.D. scholarship (2011-2014) through a competitive selection process. Earlier in 2006 he was a Summer Intern with the Cultural and Educational Technology Institute, Xanthi, Greece, whereas in 2009 he worked via the European vocational training program *Leonardo Da Vinci* in the Institute of Industrial and Control Engineering (IOC), Polytechnic University of Catalonia (BarcelonaTech), Barcelona, Spain. In 2012 he was with the Organizing Committee of the ACRI 2012 Conference, in Santorini, Greece, on 24-27 Sept. 2012, where he met with Prof. Leon Chua, the "inventor" of the memristor. A summary of his research work was selected for presentation in the Ph.D. Forum special session of the VLSI-SoC 2013 Conference, held in Istanbul, Turkey, on 7-9 Oct. 2013, where he was *runner-up* for the best Ph.D. presentation award. In 2015 he distinguished as the *Best Ph.D. Student* of the ECE Department of DUTh.

His research emphasis is on novel nanoelectronic circuits and architectures comprising memristors. Specifically, his research so far focused on the modeling and simulation of memristors, the design and simulation of analog/digital circuits, nonvolatile (multi-level) memory architectures with memristors, resistive networks and neural networks based on memristors, as well as electronic systems implementing computational models and algorithms of artificial intelligence using memristors (e.g. for maze-solving, shortest path and traveling salesman problem, etc.). In all the aforementioned research topics, he is the main author of one of the first memristor-related monographs of the literature entitled "Memristor-Based Nanoelectronic Computing Circuits and Architectures" including a foreword by Prof. Leon Chua, published by Springer in 2015, of one book chapter in "Memristor Networks" (A. Adamatzky, L. Chua, eds.), of more than 14 journal articles and of several technical papers presented in international conferences. Currently, his research endeavor is funded through a three-year CONICYT FONDECYT Postdoctorado Chilean government research grant (2015-2018) and involves the development of novel

bio-inspired and bio-mimicking memristive circuit models, memristive artificial neural processing and learning systems, and massively parallel unconventional memristive computing approaches targeting state-of-the-art nanoelectronic hardware platforms. His research interests further include modern unconventional computing, software and hardware aspects of parallel complex computational (bio-inspired) circuits and systems, cellular automata theory and applications, circuit design and simulation.

Dr. Vourkas is invited *Guest Editor* in a Special Issue of the Taylor & Francis Int. Journal of Parallel, Emergent and Distributed Systems (JPEDS) about "Advances in Memristive Networks". He is PC member of MEMRISYS 2015, MELECON 2016, and SSCI 2016 conferences. He is regular reviewer in 17 international scientific journals and 3 major international conferences. He was *invited Tutorial speaker* in the 2015 *IEEE Int. Conf. on Electronics, Circuits, and Systems* (ICECS 2015) held in Cairo, Egypt.

Selected publications

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Previous offerings of tutorials

I was main presenter of one successful half-day Tutorial in the 2015 *IEEE Int. Conf. on Electronics, Circuits, and Systems* (ICECS 2015), held in Cairo, Egypt, the flagship conference of the IEEE Circuits and Systems Society in Region 8. The Tutorial was co-presented by Prof. Georgios Ch. Sirakoulis from the Democritus University of Thrace (DUTh) in Greece, ex-supervisor of my Ph.D. Thesis. The title of the Tutorial was "Memristive electronic computing circuits, systems and architectures" and it aimed to provide a comprehensive study spanning from memristor theory, device modeling and complex device interconnections, to circuit-level and system-level digital/analog computing applications. Among the rest of the ICECS 2015 Tutorials, our Tutorial was very well received by the ICECS attendees with an average of twenty people constantly present during our interactive presentation, being mostly M.Sc. and Ph.D. students who discussed with us several things during the break and after the presentation. Based on that previous base material, this proposed new LASCAS Tutorial will cover more recent results in memristor modeling including stochastic behavior, multi-level tuning approaches, emulating strategies, as well as more details on in-memory logic circuits and neural/neuromorphic computing approaches towards HW accelerators and learning systems, thus covering a much broader set of fundamental stuff and also major emerging applications.

Learning objectives

The topic of the proposed Tutorial falls in the area of cutting-edge research and development topics, namely that of emergent computing device technologies, circuits and system architectures. Its main objective is to provide a comprehensive study of this research area which spans from memristor fundamental theory, device modeling/emulating details and composite device interconnections, to circuit-level and system-level digital/analog implementations for in-memory computing and learning. It includes several new results originating from the research endeavor and collaborative activities of the presenter in this very promising and highly multidisciplinary scientific field. At the moment and to the best of my knowledge, there is not any similar tutorial given, nor there has been any in the previous versions of the LASCAS conference, which deals with such an extended range of the provided here memristor-related research information. Consequently, **Memristor Device Modeling and Applications in Memory, Logic, Computing and Learning** can be considered a really valuable Tutorial for the attendees of LASCAS. Graduate students will learn about state-of-the-art research in such a hot technological topic and hear about the major challenges; valuable food for thought for those who consider pursuing postgraduate studies later. Likewise, postgraduate students and researchers working or willing to work in this area, will learn useful details and thus be able to soon define critical directions in their research trajectory to work on and contribute in areas with several still open problems. They will also possibly receive new information about applications of memristors which they had not heard about and find both theoretical and practical material (such as memristor models, simulation tools, emulator implementations, etc.) to potentially use, build upon, or compare with their own research results. Furthermore, academics in engineering and applied science faculties will be able to hear and discuss on material potentially useful to them to incorporate in their relevant graduate and postgraduate University courses.

Target audience and prerequisite knowledge of audience

Target audience is in fact unlimited, depending only on the willingness and passion to learn about stuff related to emerging circuit nanotechnologies. The topic of the proposed Tutorial falls within one of the areas of major interest to the CAS Community and conferences such as LASCAS always attract an important number of postgraduate students, apart from researchers and academics. Moreover, the joint organization of the IBERCHIP workshop, a forum to exchange experiences and share knowledge among academic and industrial researchers, along with the PRIME conference which is particularly focused on Ph.D. students and early-stage post-docs, add much to this. In general, students, researchers, and academics with electrical/electronic engineering, applied sciences, physics and/or computer science background knowledge, as well as people from semiconductor industry, could attend in this Tutorial.

Full Description

Since the beginning of my Ph.D. studies on Nov. 2010 up to now, my research activities broadly cover the highly interdisciplinary and emerging scientific field of nanoelectronic circuits, systems and computing architectures based on novel resistive-switching electronic devices known as “memristors” (concatenation of memory and resistors). The memristor is a two-terminal electronic device, defined by a state-dependent Ohm’s law; its resistance depends on a set of internal state-variables. Memristors received much attention worldwide from several research groups and the semiconductor industry only after 2008, when the Hewlett-Packard Laboratories announced the implementation of their first solid-state memristor prototype, thus linking Leon Chua’s 1971 theory with practice for the first time. This is a really timely research area; the first experimental memristive devices and integrated memristive memory chips have only recently reached the market, whereas more are predicted to soon be commercially available.

Currently there is a notable variety of systems that exhibit memristive behavior, promising to offer several advantages such as nonvolatility, rapid switching, low power consumption and BEOL compatibility with CMOS technology. Additionally, memristors provide an unconventional computation framework which combines information processing and storage in the memory cell itself; the major distinction from the present Von Neumann computing paradigms. Such favorable performance characteristics justify the recent explosive growth of research efforts which led to several advancements in theory and applications of memristor, rendering it a candidate alternative technology able to bring the next technological revolution in electronics, being also a bridge between CMOS and the realm of nanoelectronics.

The **Memristor Device Modeling and Applications in Memory, Logic, Computing and Learning** Tutorial brings together a series of cutting edge memristor-related research topics, i.e. device fundamental theory and modeling, emulating processes, emerging computation through complex device interactions, logic and memory circuits, as well as unconventional (brain-inspired) computing circuits and learning systems, where the memristors are used either as two-state resistive switches or as true analog elements. More specifically, the presentation consists of ten separate sessions (see tentative outline below), organized in three major parts; namely "Memristor Theory", "Memristor-based Logic and Memory Circuits" and "Memristor Applications in Computing and Learning". At the beginning we deal with the

foundations of memristor theory and the fundamental properties of memristors. Then a considerable part of the tutorial is devoted to modeling of voltage-controlled bipolar memristors and discusses state-of-the-art models which incorporate newly observed features concerning variability and stochasticity in switching behavior. This part also describes a threshold-type SPICE-compatible device model, on which the presented simulations and most of the research findings are based. Moreover, the focus is on complex memristor interactions and on the composite emerging behavior with application in memristive quantized conductance (multi-state) switches for multi-level storage cells. This first part of the Tutorial is concluded with a reference to emulating strategies for memristors, an important topic of practical research useful to engineering students and researchers who do not have access to experimental memristor devices.

Afterwards, the second part first addresses the most well known design strategies for digital logic circuits with memristors, passing from sequential stateful logic to circuit design schemes which allow for parallel processing of the applied inputs, presenting a short comprehensive comparison of them. Then the nanocrossbar-based information storage systems are introduced, studying alternative memory cells and architectural aspects which could lead to more reliable memristor-based nonvolatile random access memories. A corresponding GUI-based educational simulation tool is here presented, developed by the presenter, to be potentially considered in their early research steps in the memristive crossbar geometry and/or in relevant university class student projects. In the same context, multi-state tuning approaches are discussed and the memristive multi-state switches earlier described are here integrated with the crossbar circuit geometry in a multi-level memristor-based crossbar memory, which is then proposed as an early approach to memristor-based high-radix arithmetic logic units (ALU).

Gradually moving from circuits to systems, the last part of the Tutorial involves emerging parallel computing capabilities of complex 2D memristor networks. It presents a novel methodology to efficiently map oriented graphs onto memristive networks, using circuit models which cover a variety of connection types between graph vertices. Also, a circuit-level, Cellular Automata (CA)-inspired methodology for computational schemes which are applied to solve several NP-hard problems of various areas of artificial intelligence (AI), is presented. Finally, this Tutorial is concluded with a reference to one of the most promising applications of memristors, i.e. neural/neuromorphic computing and learning systems, with impressive simulation results.

Tentative Outline of the 10 Major Sessions

1. Memristor Fundamentals
2. Memristor Devices, Behavioral Models, and Variability-Stochasticity characteristics
3. Dynamic Response of Multiple Interconnected Memristors
4. Memristor Emulators
5. Memristor based Logic Circuits
6. Memristor Crossbar-based Nonvolatile Memory
7. Multi-level Memristor Tuning and Multi-level Memory Cells for High-Radix ALUs
8. Memristive Networks
9. Memristive Computing Systems for NP-Hard Problems
10. Neural/Neuromorphic Computing and Learning Systems